**EAST WEST UNIVERSITY**

**Department of Computer Science and Engineering  
  
Semester:** Spring 2017  
**Course Number:** CSE345  
**Course Title:** Digital Logic Design

**Experiment Number:** 03  
**Experiment Title:** Behavioral Verilog Simulation of a Combinational Logic Circuit

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**Date of Performance:** October 23, 2017

**Objectives**

1. To learn behavioral Verilog coding of a combinational logic circuits using procedural model.
2. To learn behavioral Verilog coding of a combinational logic circuits using continuous assign statement.

**Answers to the Pre-Lab Questions**

1. **Behavioral Verilog code by using Procedural Model**

S= A'B'C+ A'BC'+ AB'C'+ ABC

module expt3\_1(input A, B, C,   
 output reg S);  
 always @(A, B, C) begin  
 S=0;  
 if (~A & ~B & C) S=1;  
 if (~A & B & ~C) S=1;  
 if (A & ~B & ~C) S=1;  
 if (A & B & C) S=1;  
 end  
endmodule

1. **Behavioral Verilog code by using Continuous Assign Statement:**

S= A'B'C+ A'BC'+ AB'C'+ ABC

module expt3\_2 (input A, B, C,   
 output S);  
 assign S=(~A &~B & C) | (~A & B & ~C) | (A & ~B & ~C) | (A & B & C);

endmodule